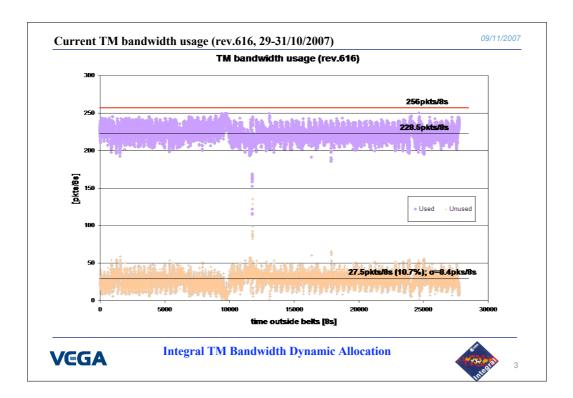
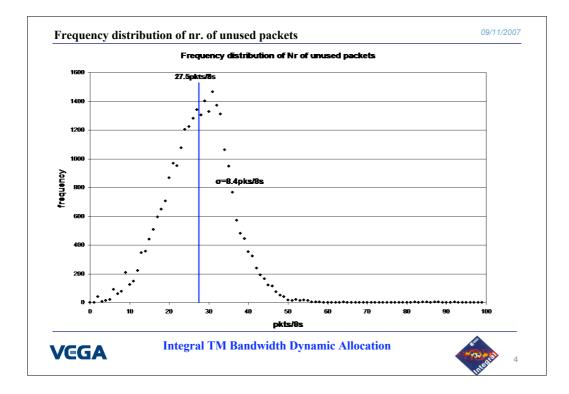


 The problem TM bandwidth of Integral is 256pks/8s 				
TM bandwidth of Integral is 256pks/8s.				
(TM pkts are 448bytes fixed length in Integral)				
• The allocation among the subsystems is the fol	lowing:			
− 246 P/L (96 fixed + 150 programmable) \rightarrow	IBIS	128		
 2 CDMU (1HK pkt + 1Report pkt) 	SPI	105		
 4 AOCS (3HK pkts + 1Report pkt) 	JEM-X1	8		
 3 RTU HK pkts 	JEM-X2	0		
 1 Memory Dump pkt 	OMC	5		
 As packet acquisition is based on fixed PST pr bandwidth resource usage is <i>in-efficient</i> → If a transmit that bandwidth is lost. 	0	1	,	
• At present the average unused bandwidth is ab	out 27.5pkts/	/8s (~11%)).	
VEGA Integral TM Bandwidth Dynar	nic Allocation	1	d'	





09/11/2007 **Possible solutions** • To exploit the unused TM packets, a more clever packet acquisition mechanism is needed on-board. The static PST mechanism - implemented by the CDMU Standard Application Software (SASW) - needs to be enhanced to dynamically re-allocate unused packets. The allocation algorithm must be such that the nominal P/L bandwidth share (i.e. currently 128,105,8,0,5 pkt/8s) is always granted. Possible algorithms are (just for example): If a PT does not have any packet to transmit in a PST slot, then that PT is no more a) polled/or polled less frequently till the end of the TM cycle and the unused PST slots re-programmed on-the-fly to other PTs. b) At a given TM cycle, the nr of the previous cycle unused PST slots of a PT is transferred to other PTs less one packet. Should that packet be used, then at the next cycle the nominal allocation is restored. Allow the PTs to acquire all-together more than 256pkts and stop the acquisition when c) that limit is reached (but ways to ensure nominal share to be studied). **Integral TM Bandwidth Dynamic Allocation** VEGA

CI	DMU SASW change	09/11/200
•	These algorithms can be implemented modifying existing SASW mechanisms, e.g.	:
	- Modify PST mechanism	
	 PST slots reprogrammed either on-the-fly or on the shadow-programmable PST, act the next TM cycle. 	tivated at
	 Modify BRAT mechanism 	
	• Over-allocate PST TM slots (>256) to PTs, using subset of TC_SEND (~40) and NO_TRANS (14) slots and if needed RTU slots (~18) and	
	 introduce a new BRAT control to limit the total amount of bandwidth (<!--=256 pack<br-->instead of limiting the bandwidth of a single PT. 	ets)
•	Other problems to be studied:	
	- Rules and constraints on PST slots must be now hardcoded in the SASW	
	 Change of RTU packets closure mechanism if we want to free additional slots. 	
	 Ensure nominal share and priority rules to re-assign the unused bandwidth. 	
	 Interfaces in the planning system and monitoring of dynamic allocation in TM. 	
	 Compatibility of the selected option with instrument DPE software. 	
	- CDMU additional CPU load and memory to be evaluated.	
•	Performances could be further improved by exploiting the CDMU TM buffer (175 today running basically empty, to accommodate P/L TM peaks on VC7.	pkts),
	- For instance bandwidth control (=256) can start when 80% of buffer used by VC7.</td <td></td>	
V	EGA Integral TM Bandwidth Dynamic Allocation	Alegran (

