Integral PST Over-allocation – The problem.

- Periodic saturation of downlink Bandwidth assigned to individual PTs, causing some observations to be compromised.
- In particular SPI affected.
- Instruments use Bandwidth inefficiently due to fixed PST.
  - Even if spare BW is available it is not reallocated dynamically to PTs which are saturated.
  - Individual PTs saturate their BW only part of the time.
  - PTs saturate their BW simultaneously only occasionally and briefly.
  - Close to RT re-programmation of PST by ground is difficult and would probably need dedicated S/W.
- Total Downlink BW is 256 Packets / TM Cycle.

Integral PST Over-allocation – Old BW Allocation.

- BW Allocation (TM Packets).
  - CDMU 5 (1xCDMU HK, 3xRTU, **1x Occasional Report**).
  - Acc 4 (3xHK, **1x Occasional Report**).
  - Patch & Dump 1 (**1x Occasional Report**).
  - PLM 246 (96 fixed – IBIS: 90, SPI: 5, OMC: 1, 150 Programmable by ISOC)
  - Total 256.
- 3 Occasional Report packets used infrequently
- CDMU Buffering facilities (175 packets) not used.

Integral PST Over-allocation – Old BW Usage.

- Over 8 sample revolutions (observations: Crab, GRS 1915+105, Gal. Disk, Gal. Plane Region 1, mid-latitude 1, OMC FF, Gal. Plane Reg. 2)
  - 5863 cycles (2.5%) with report packets, 1094 with 2 report packets (ACC + CDMU).
  - **No TM cycles containing 3 report packets**.
  - No instances of successive TM cycles containing report packets except during one period of 20 JEM-X2 memory dump packets.
  - 1135 instances where 2 report packets were received within 3 cycles.
- The number of report packets which can be generated per cycle is limited to 1 of each type on board.
- These 3 windows could probably be double allocated in the PST by increasing the PST allocation to SPI and maintaining the current OR TM bandwidth PST allocation.

Integral PST Over-allocation – New BW Allocation.

- BW Allocation (TM Packets).
  - CDMU 5 (1xCDMU HK, 3xRTU, 1x Occasional Report).
  - Acc 4 (3xHK, 1x Occasional Report).
  - Patch & Dump 1 (1x Occasional Report).
  - **PLM 249 (99 fixed – IBIS: 90, SPI: 8, OMC: 1, 150 Programmable by ISOC)**
  - **Total 259.**
- 3 Occasional Report packets used infrequently
- CDMU Buffering facilities used occasionally.
- Tested during Revolutions 631, 632, 633, 637, 647, 649, 650

Integral PST Over-allocation – Current Status.

- New BW Allocation in use:
  - Revolutions 651 to 662: new PST loaded manually whenever standard PST allocation (105, 128, 8, 0, 5) in use.
  - Since revolution 663 (18/3/2008) the new PST has been loaded via Timeline for all PST allocations specified by ISOC.
- BCPKT and MOUTs in Timeline not yet in line with new PST Allocation.
- Maximum observed CDMU TM Buffer Occupancy: 32 Packets (3/3/2008).
- No problems experienced.
- Simple CDMU TM Buffer model on MCS.

Integral PST Over-allocation – Further Over-allocation.

- Revolutions 649 to 654, TM usage data was gathered and a number of simple simulations run to try to predict the effect of further over-allocation on CDMU TM buffer occupancy.
  - Assumption: SPI would use all of any extra simulated allocation whenever it used all of its actually assigned over-allocation of 3 slots. (In practice this is unlikely to always be the case, so we are simulating assuming the worst case).

	Modelled Maximum TM Buffer Occupancy with SPI PST Over-Allocation of:						
Revolution	**4**	**5**	**6**	**7**	**8**	**9**	**10**
649	1	2	3	4	5.2	9.2	13.2
650	1	2	3	4	6.2	10.3	17.8
651	10.7	25.2	52	85	118.2	153.2	195.5
652	1	4.2	11.5	19.5	28.7	40.9	60.2
653	4.4	11.5	19.6	32	48	80.5	120.5
654	103.2	203.2	303.3	405.3	535.3	669.3	920.7